REMARKS

Claims 1-20 are present in this application with claims 9-17 and 19 being withdrawn for being directed to a non-elected invention. Applicants reserve the right to file a divisional application directed to the non-elected invention including at least claims 9-17 and 19. Clarifying amendments have been made to claims 1 and 18. Reconsideration and allowance of the claims 1-8, 18 and 20 of the present application as amended are earnestly solicited in view of the following remarks.

Claims 1, 2, 5-8, 18 and 20 stand rejected under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent No. 6,066,547 to Maekawa in view of Muller et al. (Device Electronics for Integrated Circuits 2nd Edition) and further in view of U.S. Patent No. 3,887,993 to Okada et al. and claims 3 and 4 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Maekawa. These rejections are respectfully traversed.

Claim 1 of the present application recites a method for annealing a semiconductor structure comprising the steps of subjecting the semiconductor structure at an oscillating electromagnetic field after implanting a dopant into the semiconductor structure and then either before and/or after this step, applying a LTRTA process to the semiconductor structure. Similarly, claim 18 of the present application recites a method for processing a semiconductor structure comprising the steps of subjecting the structure to athermal heating and applying a LTRTA process thereto. Amended claims 1 and 18 recite that the utilization of electromagnetic fields or athermal heating induces current flow through the semiconductor structure to cause ohmic collisions between high energy electrons and the semiconductor lattice structure to provide rapid heating from within the structure. The LTRTA is performed to further repair the semiconductor structure and to minimize diffusion. The combination of subjecting the semiconductor to electromagnetic fields and applying a LTRTA process thereto cures structural defects, activates the dopant material, repairs the lattice structure and minimizes differences between the as-implanted junction depth and the post annealing junction depth as compared to known RTA methods. It is critical to maintain shallower junction depths in processing smaller

semiconductor devices and the methods recited in the claims of the present application are directed towards minimizing diffusion of the as-implanted junction depth.

Maekawa is relied upon to disclose a method for annealing amorphous silicon films to produce polycrystalline films suitable for thin film transistors fabricated on glass substrates. However, as acknowledged in this rejection, Maekawa does not disclose the purpose of applying an LTRTA process to the semiconductor structure as claimed in the present application. Therefore, Muller et al. are relied upon in attempting to cure this deficiency. On the paragraph bridging pages 79 and 80, Muller et al. disclose that an annealing step is necessary to restore the lattice quality and to ensure that the implanted dopant atoms are located on substitutional sites and that the ions may be redistuributed by a subsequent diffusion after the ions are implanted if desired. However, Muller et al. fail to suggest or imply applying a LTRTA process either before and/or after subjecting the semiconductor structure to an oscillating magnetic electromagnetic field or athermal heating as recited in the claims of the present application. Okada et al. are further relied upon to disclose a method of making an ohmic contact simultaneous with the semiconductor substrate. In particular, Okada et al. disclose at col. 1, lines 60-65 that the junction depths should be as shallow as possible in order to realize an abrupt step-type impurity distribution but that it is difficult to connect such shallow junction with ohmic electrodes. Again, Okada et al. do not suggest or imply applying a LTRTA process either before and/or after subjecting the semiconductor structure to an oscillating magnetic electromagnetic field or athermal heating as required by the claims of the present application. Therefore, the combination of Maekawa, Muller et al. and Okada et al. do not suggest or imply the combination of subjecting the semiconductor to electromagnetic fields and applying a LTRTA process for curing structural defects, activating the dopant material, repairing the lattice structure and minimizing differences between the as-implanted junction depth and the post annealing junction depth in processing shallow junction semiconductor devices as recited in the claims of the present application.

Dependent claims 3 and 4 of the present application recite providing a frequency in the microwave frequency band and in a radio frequency band respectively. It is acknowledged in this rejection that Maekawa does not disclose providing a frequency in either a microwave frequency band or a RF band but it is alleged that it is well know to

provide any frequency range in a frequency band where needed. However, it is respectfully submitted that it would not have been obvious to provide such frequencies as higher frequency fields, such as microwave fields, can heat more efficiently than lower frequency field, such as RF fields, in some embodiments and it would not have been obvious to provide any frequency range in a frequency band where needed as alleged in this rejection. Accordingly, it is respectfully submitted that claims 1 and 18 along with their dependent claims 2-8 and 20 patentably define over the combination of Maekawa, Muller et al. and Okada et al. for at least the reasons set forth above and it is respectfully requested that these rejections be reconsidered and withdrawn.

In view of these amendments and for all of the above stated reasons, it is respectfully submitted that all of the outstanding rejections have been overcome. Therefore, it is respectfully requested that claims 1-8, 18 and 20 of the present application be passed to issue.

If any issues remain unresolved, the Examiner is requested to telephone the undersigned attorney. Please charge any additional fees or credit any overpayments to deposit account No. 50-0896.

Respectfully submitted,
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